



Figure 2A. DIP Connections

32 VCC Vpp [1 31 **h** ₱ A16 **[**2 A15 1 3 30 J NC

A12 🕇 4 29 A14 28 h A13 **A7** A6 27 h A8

A5 **f** 7 26 A9 25 A11 A4 **f** 8 M27C1001 A3 24 **h** G A2 1 10 23 A10

22 **h** E A1 [11 A0 **f** 12 21 ll Q7 Q0 f 13 20 D Q6 Q1 f 14 19 h Q5 Q2 1 15 18 DQ4

17 h Q3

AI00711

V_{SS} [16

Table 1. Signal Names	
A0-A16	Address Inputs
Q0-Q7	Data Outputs
Ē	Chip Enable
G	Output Enable
P	Program
V _{PP}	Program Supply
Vcc	Supply Voltage
V _{SS}	Ground
NC	Not Connected Internally

Description of mounting Adaptor between 27C1001 Eprom and Socket as Replacement for TC531000 masked ROM in

All related Parts from Datasheets and details from circuitplans are displayed here to for documentation.

solder a thin coated wire to Pin 22 of the socket and place the rest of the wirepart up to the frontend at Pin1 with enogh left wire to later connect this open end to

Place a 28pin Socket firmly at your solderingplace.

Pin 2 of the programmed Eprom. Carefully bend Pin 2, Pin 32 and Pin30 and Pin 24 to horizontal position away from the programed chip without breaking the pins (according to upper middle drwaing).

into the Socket with the remaining 4 Pins (1,2,31 and 32) "hangover" the top of the socket. Carefully solder short piece of wire from Pin 22 of the programed Eprom (that is inserted at Pin 20 of the

from Pin 20 of the socket to Pin 2 of the Eprom. Finished!

Plugin the programed Eprom with the Pins 3 to 16 and Pins 17 to 30

socket) to Pin 24 of the Eprom too. Connect remaining end of the wire

Important remark: make sure there is NO contact between pin 24 of the Eprom and pin

They might be removed from Marked Pins without use at Adaptor! programed Eprom!

Lineconnections between Eprom and socket 28 pin Socket 32 31 30 28 27 29 **h** 2 3 26 28 27 25 24 23 24 21 23 20 22 10 19 21 18 20 **b** 12 17 19 13 16 18 **h**

15

22 of the socket !!!

explosiondrawing of Eprom-pins

ri 16

Apple IIGS ROM 0 or ROM 1 models Solder short wire from pin 28 of socket to pin 32 of Eprom.

O²

128KX8

Apple IIGS

VCC

A14

A13

A8

A 9

A11

A10

Q7

- Q6

- Q5

Q4

Q3

A16 RomOE

CS ROMSEL

LACHSEL.L 1

ROMOE/A16 1

28

27

26

25

24

22

21

20

19

18

17

16

15

20 CE/CE

19 D7

Apple ROM0/ROM1

TC53100

A15

A12

A 7

A 6

A 5

A 4

A 3

A 2

A 1

A 0

Q0

Q1

Q2

VSS

10

12

13

11

PIN CONNECTION 28 1 VDD A15 🗗 A1 2 d2 27 A14 A7 d3 26 A13 A6 🗗 4 25 A 8 24 A A 9 A5 🗖 5 23 A1 I A4 🗆 6 22 A 16 A3 🗖 7 21 A 10 ∧2**□**8

> DO C 11 18 D D6 17 D D5 D1 d12 D2 🗖 13 16 D4 GND□14 15 D D3

A1 🗗 9

A0 | 10

PIN NAMES	
A0 ~ A16	Address Inputs
D0 ~ D7	Data Outputs
CE/CE	Chip Enable Input
VDD	Power Supply
GND	Ground